

HNS P-Channel Enhancement Mode Power MOSFET

Description

The HNS6012A uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is well suited for high current load applications.

General Features

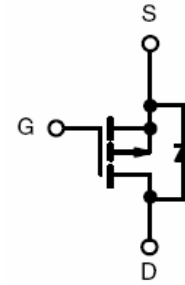
- $V_{DS} = -60V, I_D = -12A$
 $R_{DS(ON)} < 100m\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} < 125m\Omega @ V_{GS} = -4.5V$
- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- High side switch for full bridge converter
- DC/DC converter for LCD display

100% UIS TESTED!

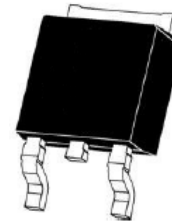
100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment



TO-252 -2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HNS6012A	HNS6012A	TO-252-2L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-12	A
Drain Current-Continuous($T_C = 100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	-8.5	A
Pulsed Drain Current	I_{DM}	-30	A
Maximum Power Dissipation	P_D	60	W
Derating factor		0.4	W/ $^\circ\text{C}$
Single pulse avalanche energy (Note 5)	E_{AS}	50	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

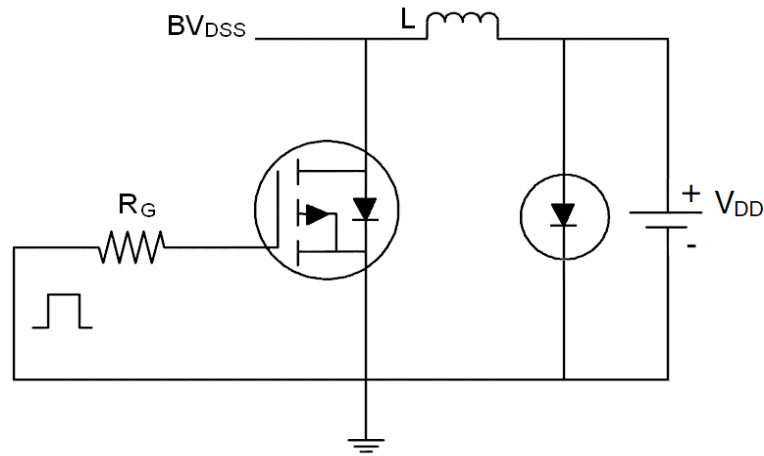
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V, V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1	-1.5	-2.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-12A	-	84	100	mΩ
		V _{GS} =-4.5V, I _D =-8A	-	100	125	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-12A	-	10	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =-30V, V _{GS} =0V, F=1.0MHz	-	1630.7	-	PF
Output Capacitance	C _{oss}		-	90.6	-	PF
Reverse Transfer Capacitance	C _{rss}		-	77.3	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-30V, R _L =1.5Ω, V _{GS} =-10V, R _G =3Ω	-	11	-	nS
Turn-on Rise Time	t _r		-	14	-	nS
Turn-Off Delay Time	t _{d(off)}		-	33	-	nS
Turn-Off Fall Time	t _f		-	13	-	nS
Total Gate Charge	Q _g	V _{DS} =-30, I _D =-12A, V _{GS} =-10V	-	37.6		nC
Gate-Source Charge	Q _{gs}		-	4.3		nC
Gate-Drain Charge	Q _{gd}		-	7.2		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =-12A	-		-1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	-12	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =- 12A di/dt = -100A/μs ^(Note3)	-	35		nS
Reverse Recovery Charge	Q _{rr}		-	38		nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

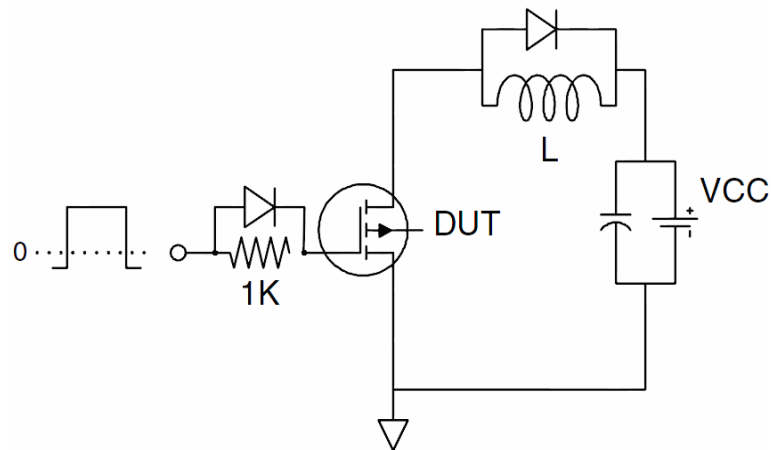
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: $T_J=25^{\circ}\text{C}, V_{DD}=-20V, V_G=-10V, L=1mH, R_G=25\Omega$

Test Circuit

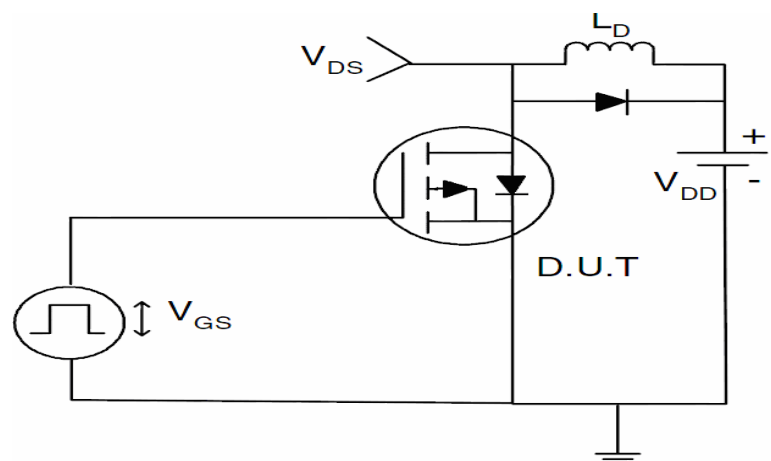
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

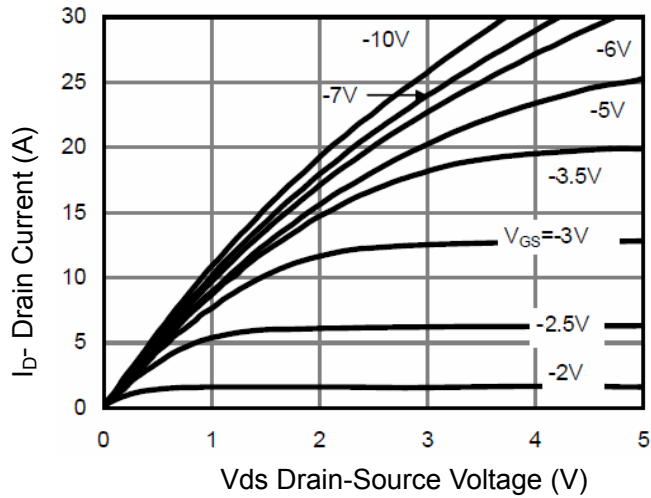


Figure 1 Output Characteristics

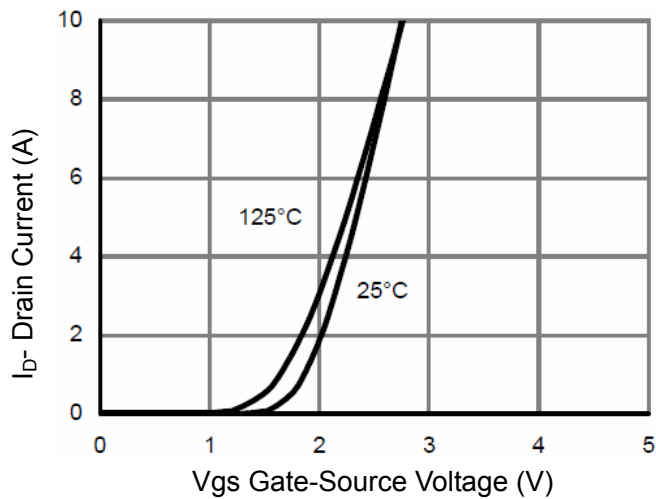


Figure 2 Transfer Characteristics

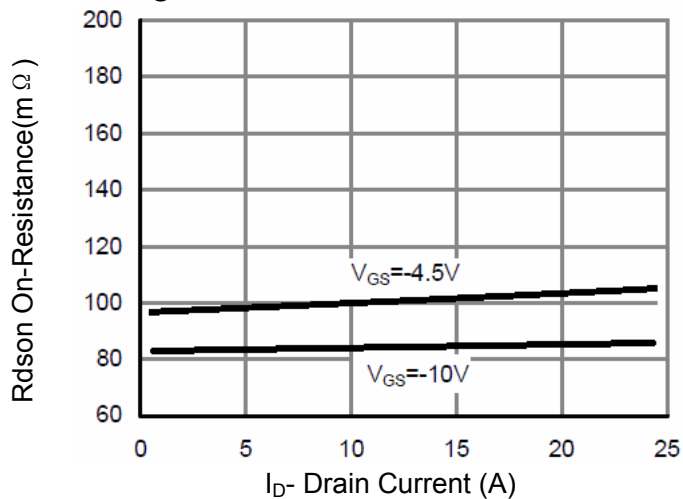


Figure 3 $R_{DS(on)}$ - Drain Current

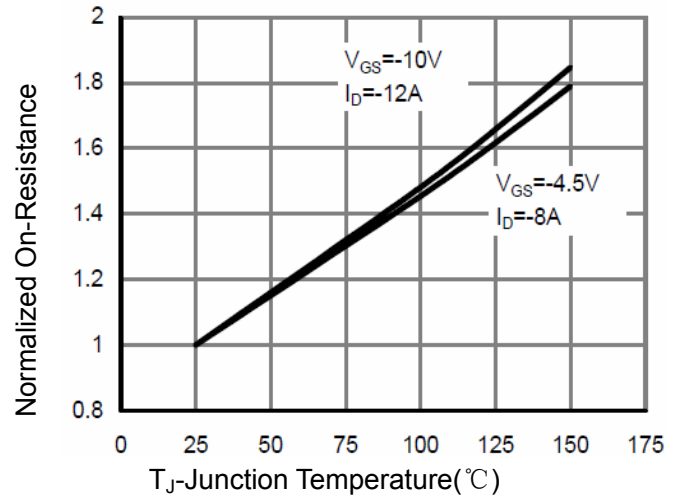


Figure 4 $R_{DS(on)}$ -Junction Temperature

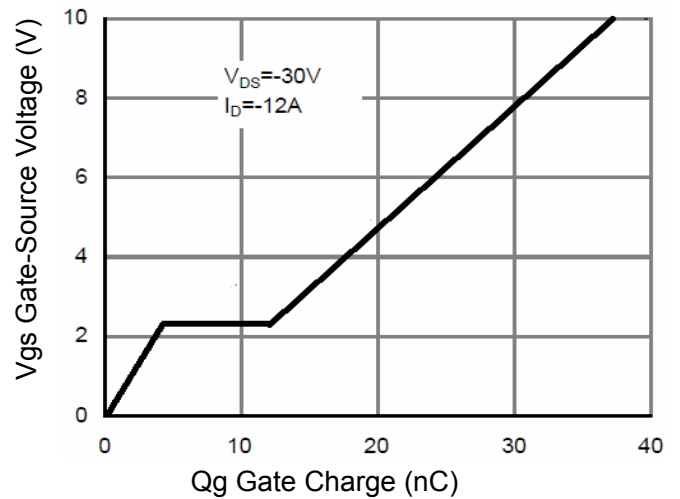


Figure 5 Gate Charge

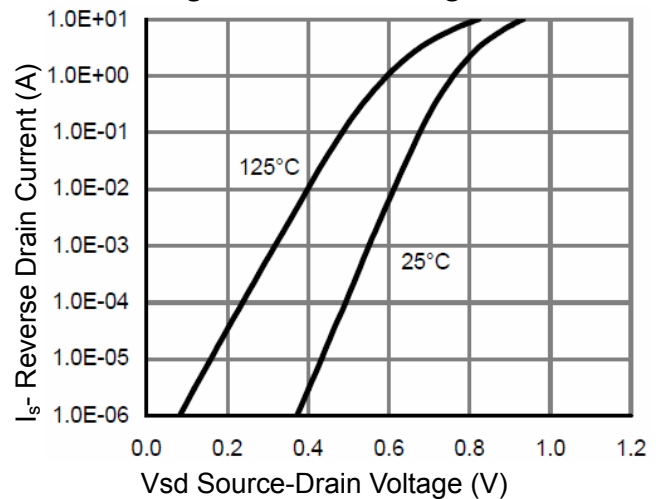


Figure 6 Source- Drain Diode Forward

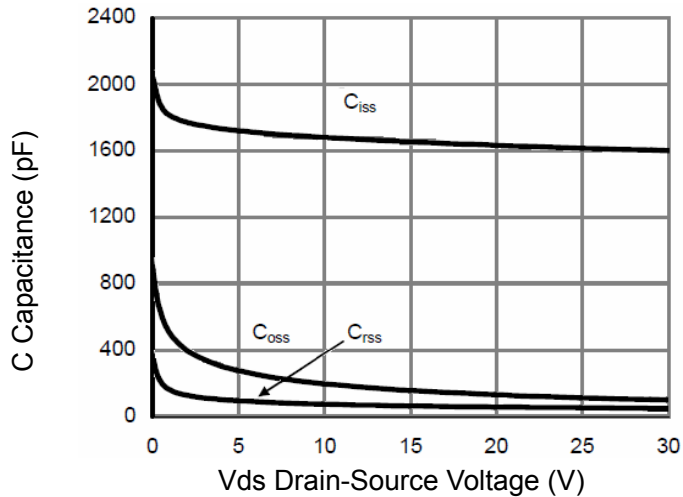


Figure 7 Capacitance vs Vds

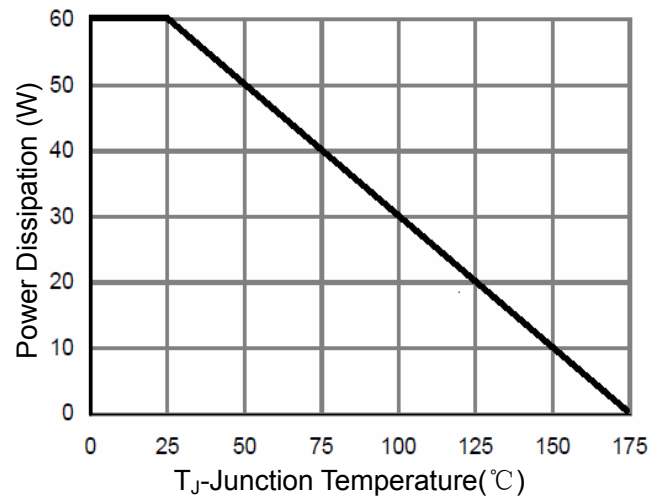


Figure 9 Power De-rating

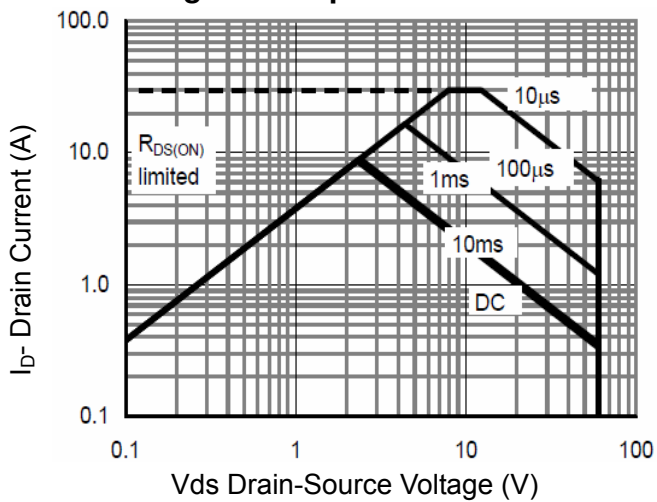


Figure 8 Safe Operation Area

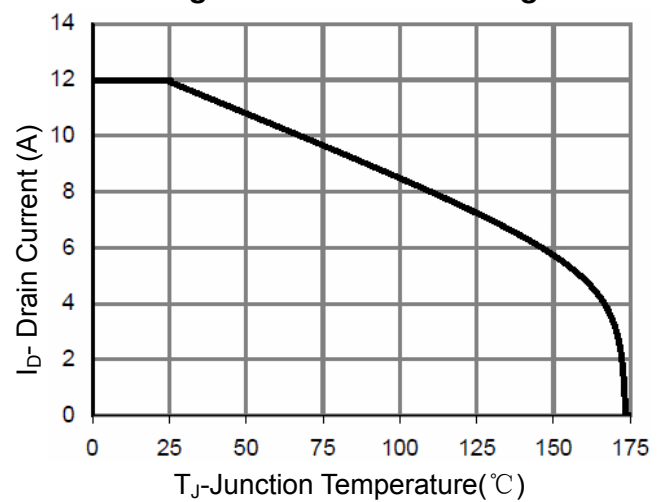


Figure 10 ID Current De-rating

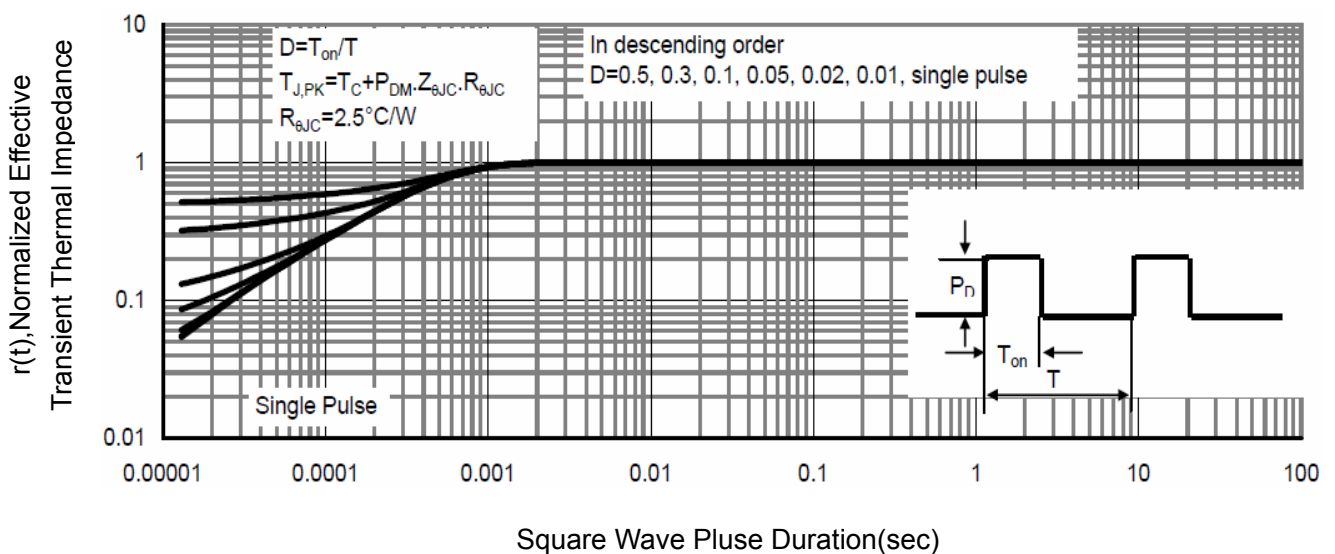
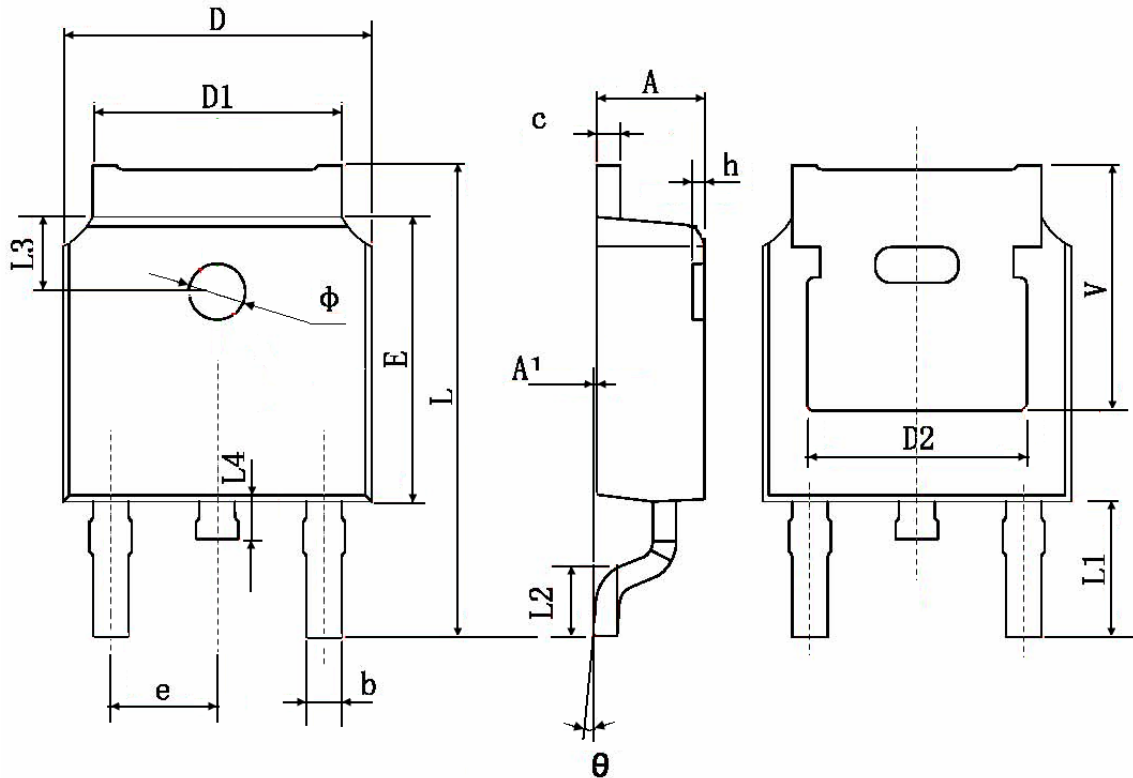


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	